II. Art Rejections:

Claims 43-57 have been rejected under 35 U.S.C. § 103(a) over Grivna et al. (U.S. Patent No. 5,641,712). This rejection is overcome for at least the following reasons.

Grivna et al. relates to a method and structure for reducing capacitance between interconnect lines (11, 24, 26) utilizes air gaps (17, 47) between the interconnect lines (11, 24, 26). Deposited over the interconnect lines (11, 24, 26), a silane oxide layer (14) forms a "breadloaf" shape which can be sputter etched to seal the air gaps (17, 47). Prior to the deposition of the sputter etched silane oxide layer (14), spacers (13, 42, 43) can be formed around the interconnect lines (11, 24, 26) to increase the aspect ratio of gaps (23, 31) between the interconnect lines (11, 24, 26) which facilitates the formation of the "breadloaf" shape of the silane oxide layer (14).

Given the disclosure contained therein, Grivna et al. fails to disclose or suggest a pre-cursor to a semiconductor device that contains therein at least one area of sacrificial material that is greater in height than a neighboring area of second material and/or conductive material.

Since the cited art fails to disclose or suggest the claimed pre-cursor to a semiconductor device, the cited art cannot render obvious claims 43-57. Accordingly, claims 43-57 are patentable over the art made of record and withdrawal of the pending rejection is respectfully requested.

III. Conclusion:

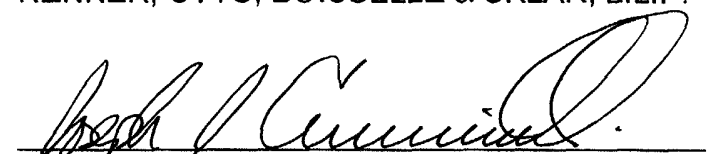
For at least the above reasons, withdrawal of the pending rejection and allowance of claims 43-57 is respectfully requested.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account No. 18-0988, Attorney Docket No. **BFGBP0217USA**.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, L.L.P.



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APPENDIX

Below is a detailed listing of the changes made to the claims. Please note, underlining denotes additions and [~~bracketed strikeout~~] denotes deletions.

In The Claims:

Claims 43 and 56 have been amended as follows:

43. (Amended) A pre-cursor to a semiconductor device containing at least one [~~air gap~~] area of sacrificial material made in accordance with a method comprising the steps of:

(A) forming a patterned layer of sacrificial material on a substrate corresponding to a pattern of one or more gaps to be formed in the semiconductor structure;

(B) depositing a second material on the substrate within regions bordered by the sacrificial material with the second material being formed with a height less than the height of the adjacent sacrificial material; and

(C) forming an overcoat layer of material overlying the patterned layer of sacrificial material and second material in the regions bordered by the sacrificial material[~~;~~

~~(D) causing the sacrificial material to decompose into one or more gaseous decomposition products; and~~

~~(E) removing at least one of the one or more gaseous decomposition products by passage through the overcoat layer so that one or more air gaps are formed within the semiconductor structure~~],

whereby the height of the one or more [~~air gaps~~] areas of sacrificial material exceeds the height of the one or more areas of second material.

56. (Amended) A pre-cursor to a semiconductor comprising:

a substrate;

a patterned layer of conductive material on the substrate;

a patterned layer of sacrificial material on the substrate, the patterned layer of sacrificial material being greater in height than the patterned layer of [~~having one or more air gaps surrounded by the~~] conductive material; and

an overcoat layer of a material overlying the patterned layer of conductive material and the [~~one or more air gaps;~~] patterned layer of sacrificial material[

~~wherein the one or more air gaps have a height which exceed the height of the relatively adjacent portions of the conductive material~~].